CLAIMS

What is claimed is:

1. A memory module comprising:

a plurality of memory devices; and

a memory module controller configured to receive a memory transaction from a first memory bus and to control access to the plurality of memory devices.

2. The memory module of claim 1, wherein the memory module controller receives the memory transaction in a first format and reformats the memory transaction into a second format, the memory module controller providing the reformatted memory transaction to at least one of the plurality of memory devices.

3. The memory module of claim 1, further comprising a second memory bus coupled between the memory module controller and the plurality of memory devices.

4. The memory module of claim 3, wherein the second memory bus comprises separate address, data, and control signal lines.

5. The memory module of claim 1, wherein the second memory bus comprises a clock signal.

6. The memory module of claim 1, wherein the first memory bus operates at a first data rate and the second memory bus operates at a second data rate, wherein the first data rate is different than the second data rate.

7. The memory module of claim 1, wherein the first memory bus has a first number of signals lines and the second memory bus has a second number of signal lines, wherein the first number of signal lines is different than the second number of signal lines.

8. The memory module of claim 1, wherein the memory module controller comprises:

request handling circuitry structured to receive the memory transaction from the first memory bus; and

control logic coupled to the request handling circuitry and reformatting the memory transaction, the memory module controller providing the reformatted memory transaction to at least one of the plurality of memory devices.

9. The memory module of claim 1, wherein the first memory bus carries time-multiplexed data and address information, and the second memory bus includes separate address and data lines.

10. The memory module of claim 1, wherein the memory module is a dual in-line first memory module (DIMM).

11. The memory module of claim 1, wherein the memory module is a single in-line first memory module (SIMM).

12. The memory module of claim 1, wherein the plurality of memory devices comprise volatile memory devices.

13. The memory module of claim 1, wherein the plurality of memory devices comprise nonvolatile memory devices.

14. The memory module of claim 1, wherein the memory module controller generates a handshake signal that indicates when the memory module controller is communicating data to the system memory controller.

15. The memory module of claim 1, wherein the memory transaction is a write transaction.

16. The memory module of claim 1, wherein the memory transaction is a read transaction.

17. A memory module comprising:

a plurality of memory devices; and

a memory module controller coupled to a plurality of memory devices, wherein the memory module controller receives a first memory transaction from the memory bus in a first format and provides a second memory transaction in a second format to at least one of the second plurality of memory devices.